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10/625,902	07/24/2003	Hideyuki Otake	OKI.556	1200

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EXAMINER	
JEANGLAUDE, JEAN BRUNER	
ART UNIT	PAPER NUMBER
2819	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/625,902	OTAKE, HIDEYUKI	
	Examiner	Art Unit	
	Jean B. Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE filed on 12-13-06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3, 5, 7, 8, 10, 14, 22 - 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 5, 7, 8, 10, 14, 22 - 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response To The Amendments/Arguments

Applicant's arguments with respect to claims 1, 3, 5, 7, 8, 10, 14, 22- 26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 3, 5, 7, 8, 10, 14, 22 - 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brunolli et al. (US Patent Number 6,201,491) in view of Ginetti (US Patent Number 5,831,566).

2. Regarding claims 1, 22, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) comprising: a first potential terminal (V_{CC}) for supplying a first potential; a second potential terminal (the ground) for supplying a second potential; an output node (output) for outputting an analog signal (figs. 3, 5) ; a first resistor circuit (302, fig. 3; 902, fig. 5) having a plurality of first resistors connected in series between a first node and the output node through a plurality of first connecting points (figs. 3, 5); a second resistor circuit (306, fig. 3; 906, fig. 5) having a plurality of second resistors connected in series between a second node and the output node through a plurality of second connecting points (figs. 3, 5) in which the first potential is a reference potential (Vcc =Vref) and the second potential is a ground potential (ground) (col. 6, lines 17, 18). Brunolli et al. does not specifically disclose a digital-to-analog converter that comprises

a first switching circuit including P-channel type MOS transistors each of the P-channel type MOS transistor connected directly to the first potential terminal, and to respective ones_of the first connecting points and the first node wherein only the P-channel type MOS transistors are connected to the first resistors as switches; a second switching circuit including N-channel type MOS transistors each of the N-channel type MOS transistors connected directly to the second potential terminal (the ground), and to respective ones of the second connecting points and the second node wherein only the N-channel type MOS transistors are connected to the second resistors as witches; and a control circuit connected to the first and second switching circuits for controlling P-channel type MOS transistors and the N-channel type MOS transistors. However, Ginetti, in a related field, discloses a low voltage DAC that comprise a first switching circuit (MP0, ..., MP3) including P-channel type MOS transistors each of the P-channel type MOS transistor connected directly to the first potential terminal (Vdd), and to respective ones_of the first connecting points and the first node wherein only the P-channel type MOS transistors are connected to the first resistors as switches (R4, R5, R6); a second switching circuit (MN0,..., MN3) including N-channel type MOS transistors each of the N-channel type MOS transistors connected directly to the second potential terminal Vss, and to respective ones of the second connecting points and the second node wherein only the N-channel type MOS transistors are connected to the second resistors as witches (fig. 2); and a control circuit (120, fig. 2) connected to the first and second switching circuits for controlling P-channel type MOS transistors and the N-channel type MOS transistors (fig. 2).. Therefore, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to modify Brunolli et al.'s system with that of Ginetti in order to decode a digital input signal to control switches.

3. Regarding claims 3, 23, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) wherein the second switching circuit (S1,...,S4) further has a an N-channel type MOS transistor connected between the second potential terminal and the output node (figs. 3, 5) [col. 4, lines 45 – 51].

4. Regarding claims 5, 24, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) wherein the control circuit includes a first decoder for controlling the P-channel type MOS transistors [the first switches] [col. 4, lines 45 – 51] and a second decoder for controlling the N-channel type MOS transistors [the second switches] [col. 4, lines 45 – 51] (col. 6, lines 6 – 16).

5. Regarding claim 8, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) comprising: a first potential terminal (V_{CC}) supplying a first potential; a second potential terminal (the ground) supplying a second potential; an output node (the output) providing an analog signal; a plurality of first resistors (302, fig. 3; 902, fig. 5) connected in series between a first node and the output node, the first resistors being connected to each other at a plurality of first connecting points (figs. 3, 5); a plurality of second resistors (306, fig. 3; 906, fig. 5) connected in series between a second node and the output node, the second resistors being connected to each other at a plurality of second connecting points (figs. 3, 5) in which the first potential is a reference potential (Vcc =Vref) and the second potential is a ground potential (ground) (col. 6, lines 17, 18).

Brunolli et al. does not specifically discloses a digital-to-analog converter that comprises a plurality *of* first switches each of which is connected directly to the first potential terminal, and to respective ones of the first connecting points and the first node, wherein only P-channel type MOS transistors are connected to the first resistors as switches; a plurality of second switches each of which is connected directly to the second potential terminal, and to respective one of the second connecting points and the second node wherein only N-channel type MOS transistors are connected to the second resistors as switches; and a control circuit connected to control the P-channel type MOS transistors and the N-channel type MOS transistors. However, Ginetti, in a related field, discloses a digital-to-analog converter (fig. 2) that comprises a plurality *of* first switches (MP0, ..., MP3) each of which is connected directly to the first potential terminal (Vdd), and to respective ones of the first connecting points and the first node, wherein only P-channel type MOS transistors are connected to the first resistors as switches (Fig. 2) ; a plurality of second switches (MN0,..., MN3) each of which is connected directly to the second potential terminal, and to respective one of the second connecting points and the second node wherein only N-channel type MOS transistors are connected to the second resistors as switches (fig. 2); and a control circuit (120, fig. 2) connected to control the P-channel type MOS transistors and the N-channel type MOS transistors (fig. 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Brunolli et al.'s system with that of Ginetti in order to decode a digital input signal to control switches.

6. Regarding claim 10, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5), further comprising an additional N-channel type MOS transistor (S1,..., S4) connected between the second potential terminal and the output node (figs. 3, 5) [col. 4, lines 45 – 51].

7. Regarding claim 12, Brunolli et al. discloses a digital--to-analog converting circuit wherein the control circuit includes a first decoder for controlling the P-channel type MOS transistor and a second decoder for controlling the N-channel type MOS transistors (col. 6, lines 6 – 16) [col. 4, lines 45 – 51].

8. Regarding claim 25, Brunolli et al. discloses a digital-to-analog converting circuit (figs. 3, 5) , wherein the first potential is a reference potential (Vcc=Vref) and the second potential is a ground potential [ground] (col. 6, lines 17, 18).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 7, 14, 21 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brunolli et al. (US Patent Number 6,201,491) in view of Ginetti (US Patent Number 5,831,566) as applied to claim 1, 8, 22 above, and further in view of Leung et al. (US Patent Number 6,400,300).

11. Regarding claims 7, 14, 21, Brunolli et al. in combination with Ginetti discloses all the limitations as discussed above except the digital-to-analog converting circuit

comprising an amplifier connected to the output node for amplifying analog signal. However, Leung et al., in a related field, discloses a DAC (figs. 1) comprising an amplifier (26) connected to the output node for amplifying analog signal (fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Brunolli et al.'s system with that of Leung et al. in order to carry out conversion process.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (See PTO-892).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jean Bruner Jeanglaude
Primary Examiner
January 2, 2007